

What is claimed is:

1. A method of forming semiconductor device, said method comprising the steps of:

5 providing a first conductive type semiconductor substrate having an epi-layer doped with impurities of said first conductive type formed thereon;

 forming a first oxide layer on said epi-layer;

 forming a nitride layer on said oxide layer;

10 patterning said nitride layer and said first oxide layer to define an active region and a termination region;

 performing ion implant to form a first doping layer of a second conductive type by using said patterned nitride layer and said first oxide layer pattern layer as an implant mask;

15 performing a thermal oxidation to form a plurality of field oxide regions into said active region and said termination region by using said patterned nitride layer and said first oxide layer as an oxidation mask;

 removing said nitride layer;

20 forming a photoresist pattern on said pad oxide layer to define a plurality of trenches in between said field oxide regions;

 recessing said epi-layer to form said trenches by using said photoresist pattern as an etch mask and said trenches spaced each other by a mesa;

 removing said photoresist pattern;

rounding corners of each said trenches by performing a thermal oxidation process and then removing all oxide layers formed thereon;

forming a barrier metal layer on sidewall surfaces, and bottom surfaces of said trenches said mesas, said field oxide regions and said
5 termination oxide regions;

performing a metallization to form a barrier metal layer on said epi-layer;

removing unreacted barrier metal layer;

forming a top metal layer on said barrier metal layer, said field
10 oxide regions and said termination region;

patterning said top metal layer to define an anode electrode;

removing layers formed on a backside surface of said semiconductor substrate during forgoing steps; and

forming a backside metal layer on said backside surface, said
15 backside metal layer acted as a cathode electrode.

2. The method according to Claim 1 wherein said first doping layer is formed by implanting both B⁺ and BF₂⁺ ion species into different depths so that a p doping layer and a p- doping layer are formed when
20 performing said step of thermal oxidation, wherein said p doping layer is positioned above said p- doping and has higher impurity concentration than said p- doping layer.

3. The method according to Claim 1 wherein said barrier metal layer is made of material selected from the group consisting of Al, AlCu,
25 AlSiCu, Ti, Ni, Cr, Mo, Pt, Zr, Co, W, Ti/TiN and the combination thereof.

4. The method according to Claim 1 wherein said top metal layer is formed of stacked layers of Al, AlCu, AlSiCu, Ti/Ni/Ag.

5. The method according to Claim 1 wherein said patterning said top metal layer comprises defining an extension portion of said top metal layer on said termination region.

6. A power rectifier device, comprising :

an n- drift layer formed on an n+ substrate;

a cathode metal layer formed on a surface of said n+ substrate opposite said n-drift layer;

10 a pair of field oxide regions formed into said n- drift layer, and said field oxide regions separated by a first mesa;

a pair of termination regions surrounded and spaced said pair of field oxide regions with a second mesa;

15 said first mesa and said second mesa having trenches formed into said n-drift layer;

a p-type doped region beneath each of said termination regions and said field oxide regions;

20 a barrier metal layer formed on sidewalls and bottom of said trenches, and formed on remnant portions of said first mesa and said second mesa; and

a top metal layer acted as an anode electrode formed on said barrier metal layer, said field oxide regions and extended to cover a portion of said termination regions.

7. The power rectifier device according to Claim 6 wherein said barrier metal layer is formed from the group of Al, AlCu, AlSiCu, Ti, Ni, Cr, Mo, Pt, Zr, and W, Ti/TiN, etc.
8. The power rectifier device according to Claim 6 wherein said top
5 metal layer is formed of stack layers of Al, AlCu, AlSiCu or Ti/Ni/Ag.